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MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

| EXAMINER |
|---|
| NGUYEN, CUONG QUANG |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/663,765 | NAM, DAE HYUN | |
| | Examiner | Art Unit | |
| | Cuong Q. Nguyen | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) *15,16,19 and 22-50* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,17,18,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-17-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restriction*

1. Applicant's election without traverse of Embodiment I, claims 1-14, 17-18 and 20-21 in Paper No. 5 is acknowledged.

### Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-4, 6-14, 17-18, and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima (US 6,420,758).

Regarding claims 1, 2, Kawachi discloses a thin film transistor in a liquid crystal display device, comprising: a first substrate (1); a crystallized semiconductor layer (a polysilicon layer 30) formed over the substrate having a channel region, a low-density impurity regions (310) and high-density impurity regions (31; a gate insulating layer (20) formed on the crystallized semiconductor layer; a first gate electrode (10) formed on the

gate insulating layer having a width corresponding to the channel region; a second gate electrode (11) formed on the first gate electrode and on the gate insulating layer such that the second gate electrode overlaps the low-density impurity regions; and a source electrode (13) and a drain electrode (12) respectively contacting the high-density impurity regions. See Kawachi et al.'s Fig.1 and Fig.2.

Regarding claims 3 and 4, the low-density impurity regions (310) (the high-resistance n-type layer) are considered as $n^-$ regions and the high-density impurity regions (31) (the low-resistance n-type layer) are considered as $n^+$ regions.

Regarding claim 6, as shown in Kawachi et al.'s Fig.1 and Fig.2, a buffer layer (21) formed on the substrate.

Regarding claims 7, 8, 9, as shown in Kawachi et al.'s Fig.1 and Fig.2, an insulating layer (22) formed over the second gate electrode, wherein the source electrode and the drain electrode are contacted to the high-density impurity regions through respective contact holes in the insulating layer; the second gate electrode layer has a width greater than a width of the first gate electrode layer; the channel region having a width corresponding to the width of the first gate electrode layer.

Regarding claims 10 and 11, as shown in Kawachi et al.'s Fig.8, Fig.9 and Fig.17, the liquid crystal display device further comprising: a second substrate (508); a plurality of gate lines (10, 11) and data lines (Vdr) formed over the first substrate so as to define a plurality of pixels; thin film transistors arranged in the plurality of pixels; a pixel electrode (14) formed in the pixel area; a color filter layer (507) formed on the

second substrate; and a liquid crystal layer (506) formed between the first substrate and the second substrate, and wherein the first gate and the second gate electrode are made of different materials (col.6, lines 18-30).

Regarding claim 12, 13, 14, 17, 18, Kawachi et al. teaches that the LCD device comprising: a first substrate (1) including a pixel area (a pixel portion as shown in Fig.9 and Fig.10) and a driving circuit area (a CMOS circuit as shown in Fig.1, Fig.12 and Fig.13); a first thin film transistor (a LDD TFT) formed in the pixel area; a second thin film transistor (an N-channel TFT) formed in the driving circuit area, the second thin film transistor including two layers of gate electrodes, a semiconductor layer (30, a polycrystalline semiconductor layer) having low-density impurity regions (310) ($n^-$ type impurity regions) overlapped with only one of the gate electrode layers, a source electrode and a drain electrode; and a third thin film transistor (an P-channel TFT) formed in the driving circuit area. See Nakajima's Fig.3A to Fig.4B.

Regarding claims 20 and 21, the rejection of claims 20 and 21 are the same as the rejection of claims 10 and 11 above.

Claims 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima (US 6,420,758).

Nakajima discloses a LCD device comprising: a first substrate including a pixel area (a pixel portion) and a driving circuit area (a CMOS circuit); a first thin film transistor (a LDD TFT) formed in the pixel area; a second thin film transistor (an N-channel TFT) formed in the driving circuit area, the second thin film transistor including two layers of

gate electrodes, a semiconductor layer (303) having low-density impurity regions (334) (n- type impurity regions. Col.10 lines 1-10) overlapped with only one of the gate electrode layers, a source electrode and a drain electrode; and a third thin film transistor (an P-channel TFT) formed in the driving circuit area. See Nakajima's Fig.3A to Fig.4B.

Claims 1-10, 12-14, 17, 20 are rejected under 35 U.S.C. 102(a) as being anticipated by Yamazaki et al. (US 6,512,271).

Regarding claims 1, 2, 5, Yamazaki discloses a thin film transistor in a liquid crystal display device, comprising: a first substrate (201); a crystallized semiconductor layer (col.8 lines 46-60) formed over the substrate having a channel region (239), a low-density impurity regions (241) and high-density impurity regions (233, 234); a gate insulating layer (206) formed on the crystallized semiconductor layer; a first gate electrode (a conductive silicon layer 113 in Fig.1B or a conductive silicon layer (a first conductive layer 207) in Fig.2A) formed on the gate insulating layer having a width corresponding to the channel region; a second gate electrode (a conductive silicon layer 115 or a conductive silicon second gate electrode 246) formed on the first gate electrode and on the gate insulating layer such that the second gate electrode overlaps the low-density impurity regions; and a source electrode and a drain electrode respectively contacting the high-density impurity regions. See Yamazaki et al.'s Fig.1A to Fig.3B.

Regarding claims 3 and 4, the low-density impurity regions (241) (N-type LDD regions) (col.11 lines 20-27) are considered as $n^-$ regions and the high-density impurity regions (233, 234) are considered as $n^+$ regions (col.11 lines 5-20).

Regarding claim 6, as shown in Yamazaki et al.'s Fig.1A to Fig.3B, a buffer layer (a base layer 202) formed on the substrate.

Regarding claims 7, 8, 9, as shown in Yamazaki et al.'s Fig.3A to Fig.3B, an insulating layer (250) formed over the second gate electrode, wherein the source electrode and the drain electrode are contacted to the high-density impurity regions through respective contact holes in the insulating layer; the second gate electrode layer has a width greater than a width of the first gate electrode layer; the channel region having a width corresponding to the width of the first gate electrode layer.

Regarding claim 10, as shown in Yamazaki et al.'s Fig.1A to Fig.4, the liquid crystal display device further comprising: a second substrate (262); thin film transistors arranged in the plurality of pixels; a pixel electrode (260) formed in the pixel area; and a liquid crystal layer (265) formed between the first substrate and the second substrate.

It is noted that , Yamazaki et al. does not explicitly show in the figures that the LCD device further comprises: a plurality of gate lines and data lines formed over the first substrate so as to define a plurality of pixels; a color filter layer formed on the second substrate. However, these elements inherently are included in Yamazaki's device because the LCD has to have these elements in order to operate.

Regarding claim 12, 13, 14, 17, Yamazaki et al.'s Fig.1A to Fig.4 shown that the LCD device comprising: a first substrate (201) including a pixel area (a pixel matrix circuit) and a driving circuit area (a CMOS circuit ); a first thin film transistor (a LDD TFT) formed in the pixel area; a second thin film transistor (an N-channel TFT) formed in the driving circuit area, the second thin film transistor including two layers of gate electrodes, a semiconductor layer having low-density impurity regions (241) ($n^-$ type impurity regions) overlapped with only one of the gate electrode layers, a source electrode and a drain electrode; and a third thin film transistor (an P-channel TFT) formed in the driving circuit area.

Regarding claim 20, the rejection of claim 20 is the same as the rejection of claim 10 above.

**Conclusion**

3. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

4. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is

(571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

6. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

Primary examiner

1/28/05